Synthesis report

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# Vivado v2021.1 (64-bit)

# SW Build 3247384 on Thu Jun 10 19:36:33 MDT 2021

# IP Build 3246043 on Fri Jun 11 00:30:35 MDT 2021

# Start of session at: Wed Apr 10 16:07:37 2024

# Process ID: 3304

# Current directory: E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/synth\_1

# Command line: vivado.exe -log UART.vds -product Vivado -mode batch -messageDb vivado.pb -notrace -source UART.tcl

# Log file: E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/synth\_1/UART.vds

# Journal file: E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/synth\_1\vivado.jou

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source UART.tcl -notrace

Command: synth\_design -top UART -part xc7z020clg400-1

Starting synth\_design

Attempting to get a license for feature 'Synthesis' and/or device 'xc7z020'

INFO: [Common 17-349] Got license for feature 'Synthesis' and/or device 'xc7z020'

INFO: [Device 21-403] Loading part xc7z020clg400-1

INFO: [Synth 8-7079] Multithreading enabled for synth\_design using a maximum of 2 processes.

INFO: [Synth 8-7078] Launching helper process for spawning children vivado processes

INFO: [Synth 8-7075] Helper process launched with PID 8000

WARNING: [Synth 8-2507] parameter declaration becomes local in uart\_rx with formal parameter declaration list [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/uart\_rx.v:9]

WARNING: [Synth 8-2507] parameter declaration becomes local in uart\_tx with formal parameter declaration list [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/uart\_tx.v:11]

WARNING: [Synth 8-2292] literal value truncated to fit in 11 bits [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/UART.v:54]

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Starting RTL Elaboration : Time (s): cpu = 00:00:03 ; elapsed = 00:00:03 . Memory (MB): peak = 1251.496 ; gain = 0.000

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INFO: [Synth 8-6157] synthesizing module 'UART' [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/UART.v:23]

INFO: [Synth 8-6157] synthesizing module 'Baud\_rate\_generator' [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/Baud\_rate\_generator.v:1]

Parameter BITS bound to: 11 - type: integer

INFO: [Synth 8-6155] done synthesizing module 'Baud\_rate\_generator' (1#1) [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/Baud\_rate\_generator.v:1]

INFO: [Synth 8-6157] synthesizing module 'uart\_rx' [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/uart\_rx.v:1]

Parameter DBIT bound to: 8 - type: integer

Parameter SB\_Tick bound to: 16 - type: integer

INFO: [Synth 8-226] default block is never used [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/uart\_rx.v:38]

INFO: [Synth 8-6155] done synthesizing module 'uart\_rx' (2#1) [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/uart\_rx.v:1]

INFO: [Synth 8-6157] synthesizing module 'seq\_mem' [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/seq\_mem.v:1]

INFO: [Synth 8-6155] done synthesizing module 'seq\_mem' (3#1) [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/seq\_mem.v:1]

WARNING: [Synth 8-7071] port 'full' of module 'seq\_mem' is unconnected for instance 'fifo\_rx' [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/UART.v:60]

WARNING: [Synth 8-7023] instance 'fifo\_rx' of module 'seq\_mem' has 8 connections declared, but only 7 given [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/UART.v:60]

INFO: [Synth 8-6157] synthesizing module 'uart\_tx' [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/uart\_tx.v:2]

Parameter DBIT bound to: 8 - type: integer

Parameter SB\_Tick bound to: 16 - type: integer

INFO: [Synth 8-226] default block is never used [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/uart\_tx.v:42]

INFO: [Synth 8-6155] done synthesizing module 'uart\_tx' (4#1) [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/uart\_tx.v:2]

INFO: [Synth 8-6155] done synthesizing module 'UART' (5#1) [E:/project final year/UART1systhesis/UART/UART/UART.srcs/sources\_1/new/UART.v:23]

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Finished RTL Elaboration : Time (s): cpu = 00:00:08 ; elapsed = 00:00:08 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:00:09 ; elapsed = 00:00:09 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Finished RTL Optimization Phase 1 : Time (s): cpu = 00:00:09 ; elapsed = 00:00:09 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.131 . Memory (MB): peak = 1496.027 ; gain = 0.000

INFO: [Project 1-570] Preparing netlist for logic optimization

Processing XDC Constraints

Initializing timing engine

Parsing XDC File [E:/project final year/UART1systhesis/UART/UART/UART.srcs/constrs\_1/imports/Downloads/Zybo-Z7-Master.xdc]

Finished Parsing XDC File [E:/project final year/UART1systhesis/UART/UART/UART.srcs/constrs\_1/imports/Downloads/Zybo-Z7-Master.xdc]

INFO: [Project 1-236] Implementation specific constraints were found while reading constraint file [E:/project final year/UART1systhesis/UART/UART/UART.srcs/constrs\_1/imports/Downloads/Zybo-Z7-Master.xdc]. These constraints will be ignored for synthesis but will be used in implementation. Impacted constraints are listed in the file [.Xil/UART\_propImpl.xdc].

Resolution: To avoid this warning, move constraints listed in [.Xil/UART\_propImpl.xdc] to another XDC file and exclude this new file from synthesis with the used\_in\_synthesis property (File Properties dialog in GUI) and re-run elaboration/synthesis.

Completed Processing XDC Constraints

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1496.027 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Constraint Validation Runtime : Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.076 . Memory (MB): peak = 1496.027 ; gain = 0.000

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Finished Constraint Validation : Time (s): cpu = 00:00:15 ; elapsed = 00:00:16 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Loading Part and Timing Information

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Loading part: xc7z020clg400-1

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Finished Loading Part and Timing Information : Time (s): cpu = 00:00:15 ; elapsed = 00:00:16 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Applying 'set\_property' XDC Constraints

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Finished applying 'set\_property' XDC Constraints : Time (s): cpu = 00:00:15 ; elapsed = 00:00:16 . Memory (MB): peak = 1496.027 ; gain = 244.531

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INFO: [Synth 8-802] inferred FSM for state register 'state\_reg' in module 'uart\_tx'

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State | New Encoding | Previous Encoding

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idle | 00 | 00

start | 01 | 01

data | 10 | 10

stop | 11 | 11

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INFO: [Synth 8-3354] encoded FSM with state register 'state\_reg' using encoding 'sequential' in module 'uart\_tx'

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Finished RTL Optimization Phase 2 : Time (s): cpu = 00:00:22 ; elapsed = 00:00:25 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start RTL Component Statistics

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Detailed RTL Component Info :

+---Adders :

2 Input 11 Bit Adders := 1

2 Input 10 Bit Adders := 6

2 Input 4 Bit Adders := 2

2 Input 3 Bit Adders := 2

+---Registers :

11 Bit Registers := 1

10 Bit Registers := 4

8 Bit Registers := 2052

4 Bit Registers := 2

3 Bit Registers := 2

2 Bit Registers := 1

1 Bit Registers := 1

+---Muxes :

4 Input 8 Bit Muxes := 1

4 Input 4 Bit Muxes := 2

2 Input 4 Bit Muxes := 3

4 Input 3 Bit Muxes := 2

4 Input 2 Bit Muxes := 2

2 Input 2 Bit Muxes := 1

2 Input 1 Bit Muxes := 25

4 Input 1 Bit Muxes := 11

3 Input 1 Bit Muxes := 4

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Finished RTL Component Statistics

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Start Part Resource Summary

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Part Resources:

DSPs: 220 (col length:60)

BRAMs: 280 (col length: RAMB18 60 RAMB36 30)

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Finished Part Resource Summary

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Start Cross Boundary and Area Optimization

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Finished Cross Boundary and Area Optimization : Time (s): cpu = 00:00:42 ; elapsed = 00:00:46 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Applying XDC Timing Constraints

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Finished Applying XDC Timing Constraints : Time (s): cpu = 00:00:47 ; elapsed = 00:00:51 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Timing Optimization

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Finished Timing Optimization : Time (s): cpu = 00:00:59 ; elapsed = 00:01:04 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Technology Mapping

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Finished Technology Mapping : Time (s): cpu = 00:01:05 ; elapsed = 00:01:09 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start IO Insertion

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Start Flattening Before IO Insertion

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Finished Flattening Before IO Insertion

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Start Final Netlist Cleanup

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Finished Final Netlist Cleanup

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Finished IO Insertion : Time (s): cpu = 00:01:09 ; elapsed = 00:01:13 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Renaming Generated Instances

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Finished Renaming Generated Instances : Time (s): cpu = 00:01:09 ; elapsed = 00:01:13 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Rebuilding User Hierarchy

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Finished Rebuilding User Hierarchy : Time (s): cpu = 00:01:11 ; elapsed = 00:01:15 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Renaming Generated Ports

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Finished Renaming Generated Ports : Time (s): cpu = 00:01:11 ; elapsed = 00:01:15 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Handling Custom Attributes

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Finished Handling Custom Attributes : Time (s): cpu = 00:01:11 ; elapsed = 00:01:16 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Renaming Generated Nets

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Finished Renaming Generated Nets : Time (s): cpu = 00:01:11 ; elapsed = 00:01:16 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Start Writing Synthesis Report

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Report BlackBoxes:

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| |BlackBox name |Instances |

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Report Cell Usage:

+------+-------+------+

| |Cell |Count |

+------+-------+------+

|1 |BUFG | 1|

|2 |CARRY4 | 4|

|3 |LUT1 | 34|

|4 |LUT2 | 71|

|5 |LUT3 | 90|

|6 |LUT4 | 39|

|7 |LUT5 | 1832|

|8 |LUT6 | 4818|

|9 |MUXF7 | 2176|

|10 |MUXF8 | 1088|

|11 |FDCE | 171|

|12 |FDRE | 16545|

|13 |IBUF | 12|

|14 |OBUF | 8|

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Finished Writing Synthesis Report : Time (s): cpu = 00:01:11 ; elapsed = 00:01:16 . Memory (MB): peak = 1496.027 ; gain = 244.531

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Synthesis finished with 0 errors, 0 critical warnings and 0 warnings.

Synthesis Optimization Runtime : Time (s): cpu = 00:00:59 ; elapsed = 00:01:12 . Memory (MB): peak = 1496.027 ; gain = 244.531

Synthesis Optimization Complete : Time (s): cpu = 00:01:11 ; elapsed = 00:01:16 . Memory (MB): peak = 1496.027 ; gain = 244.531

INFO: [Project 1-571] Translating synthesized netlist

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.194 . Memory (MB): peak = 1496.027 ; gain = 0.000

INFO: [Netlist 29-17] Analyzing 3268 Unisim elements for replacement

INFO: [Netlist 29-28] Unisim Transformation completed in 0 CPU seconds

INFO: [Project 1-570] Preparing netlist for logic optimization

INFO: [Opt 31-138] Pushed 0 inverter(s) to 0 load pin(s).

Netlist sorting complete. Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.003 . Memory (MB): peak = 1496.027 ; gain = 0.000

INFO: [Project 1-111] Unisim Transformation Summary:

No Unisim elements were transformed.

Synth Design complete, checksum: 49b138c8

INFO: [Common 17-83] Releasing license: Synthesis

29 Infos, 5 Warnings, 0 Critical Warnings and 0 Errors encountered.

synth\_design completed successfully

synth\_design: Time (s): cpu = 00:01:22 ; elapsed = 00:01:45 . Memory (MB): peak = 1496.027 ; gain = 244.531

INFO: [Common 17-1381] The checkpoint 'E:/project final year/uart\_implementation/uart\_systhesis/uart\_systhesis.runs/synth\_1/UART.dcp' has been generated.

INFO: [runtcl-4] Executing : report\_utilization -file UART\_utilization\_synth.rpt -pb UART\_utilization\_synth.pb

INFO: [Common 17-206] Exiting Vivado at Wed Apr 10 16:09:28 2024...